BioGecko Vol 12 Issue 01 2023

ISSN NO: 2230-5807

IMPLEMENTATION OF POWER GATED ALU FOR LOW POWER PROCESSOR

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ABSTRACT
Low power designs are needed not only for moveable applications, but also to lessen power in high power systems. Power consumption can be miniaturize at the system level, architectural level, algorithm level, micro-architectural level, gate level, or circuit level. Power gating of functional system has proven to be a compelling approach to cut back power consumption. With the each requirement for high speed, low power consumption, and huge performance endure to increase year after year, devices must be scaled to lower dimensionality. Current technology sees power utilization as the restraining factor. A high power supply will affect the temperature, which will affect the cooling cost of the chip. In this work the power gated ALU with minimal functions is designed and implemented. Comparison is made with presence of nmos transistor and without it. 120nm technology is employed for the design. MOS model3 parameters with 120nm technology is used in the design.1-bit ALU, 4-bit ALU and 8-bit ALU are designed and implemented with power comparisons..

KEYWORDS: POWER-GATING, ALU, LOW POWER, 120NM, MOS MODEL 3, LOW POWER PROCESSOR.

1. INTRODUCTION

With the advent of low power applications the need for effective techniques has been primary concern. Power gating is a technique used in VLSI design to reduce power consumption by turning off power to unused or idle circuits. It can be accomplished with PG cells, which reins the flow of power to certain parts of a chip. When a circuit is not in use, its power gating cell can be turned off, effectively cutting power to that circuit and reducing overall power consumption. The Power gated concept is widely employed at different sources, depending upon application type that can be Block level, Gate level/ device level. It is a widely used technique in low-power designs of processor which are used in mobile and IoT applications. Most of the Current processors employ the basic ALU which are designed & implemented using basic circuitry. They are designed to perform a wide range of operations quickly and efficiently, allowing the CPU to execute instructions and perform complex calculations. An Arithmetic Logic Unit is a digital circuit that performs arithmetic and logic operations on binary numbers. The ALU can be designed to perform a variety of operations, including addition, subtraction, multiplication, division, and logical operations such as AND, OR, and NOT. The specific design of the ALU will depend on the operations it needs to perform and the desired level of performance. the parameters are drastically changing with the advent in every year as shown in below figure

Technology year	2009	2010	2011	2012	2013	2014
Dimensions						
MPU Half-Pitch $(nm)^{\dagger}$	54	45	38	32	27	24
Physical Lgate (HP) $(nm)^{\dagger}$	29	27	24	22	20	18
Supply Voltage Parameters						
VDD (HP)†	1.00	0.97	0.93	0.90	0.87	0.84
VDD (LOP)†	0.95	0.95	0.85	0.85	0.80	0.80
Interconnect-Related Parameters						
Capacitance $(pF/cm)^{\ddagger}$	1.75	1.75	1.75	1.65	1.65	1.65
Total length $(Km/cm^2)^{\ddagger}$	2.00	2.22	2.50	2.86	3.13	3.57
Transistor-Related Parameters						
Ioff (HP) $(\mu A/um)^{\dagger\ddagger}$	0.17	0.46	0.71	0.70	0.64	0.69
Ioff (LSTP) $(pA/um)^{\dagger\ddagger}$	30.5	30.7	30.2	30.2	30.9	31.7
Cg,total (HP) $(fF/\mu m)^{\dagger}$	1.00	0.97	0.93	0.95	0.96	0.75

Figure 1: ITRS parameters for previous years.

2. LITERATURE SURVEY

Below table is some of the findings made by doing literature survey.

Table 1. Literature Survey and methods employed.

SL.NO	AUTHOR	TITLE	YEAR	CONCEPT	METHOD
1	G.SARANYA, R.S. KIRUTHIKA	Optimized Design Of An Alu Block Using Architectural Level Of Power Optimization Techniques	Mar-2011	ALU POWER REDUCTION	POWER GATING
2	N.RAVINDRAN,R.MARY LOURDE	An Optimum Vlsi Design Of 16-Bit Alu	Mar-2015	ALU POWER REDUCTION	MIXED LOGIC
3	GUANG-MINGTANG, KENSUKE TAKATA	4-Bit Slice Alu For 32-Bit Rsfq Microprocessors	Jan-2016	ALU FOR MIPS32 INSTRUCTION SET	SYNCHRONOUS CONCURRENT FLOW CLOCKING
4	JINHUI WANG, NA GONG	DCT for Low Power Microprocessors	Feb-2016	HIGHER POWER EFFICIENCY	P-TYPE/N-TYPE DYNAMIC CIRCUIT SELECTION ALGORITHM & FCR
5	YU-GUANG CHEN,WAN-YU WEN	DLRSS For Low Power Optimization	Aug-2016	EXTENSION OF DYNAMIC VOLTAGE FREQUENCY	DLRS: DYNAMIC LOGIC RECONFIGURABLE STRUCTURE

				SCALING(DVFS)	
6	CHRISTOPHER SCHAEF, JASON T STAUTH	Microprocessor Cores Stacked in Vertical Voltage using Domains Efficient Voltage Regulation	Feb-2016	EFFICIENT VOLTAGE REGUALTION	POWER CONVERSION TOPOLOGY TO MULTICORE REGULATION
7	CHENG-YEN LEE,PING-HSUAN HSIES	Stndrd Cell Design Flow Compatible Energy Recycling Logic	Jan-2016	LOW POWER	ENERGY RECYCLING MICROARCHITECTURE & ADIABATIC LOGIC
8	AN-TAI XIAO,YUNG-SIANG MIAO	A Variable Voltage Low Power Technique For Digital Circuit System	Mar-2016	LOW POWER	VOLTAGE FREQUENCY ADJUSTOR (VFA) & FREQUENCY DUTY CYCLE ADJUSTOR(FDCA) CIRCUITS
11	HAKONTOREYIN,PAMELA T BHATTI	LP ASIC Signal Processor for a Vestibular Prosthesis	Jun-2016	LOW POWER PROCESSOR	COORDINATE SYSTEM TRANSFORMATION TO CORRECT FOR MISALIGNMENT BETWEEN NATURAL SENSORS & IMPLANTED INERTIAL SENSORS

12	SMITA SINGHAL,NIDHI GAUR	Analysis & Comparision Of Leakage Power Reduction Techniques In Cmos Circuits	Sep-2015	LEAKAGE POWER REDUCTION TECHNIQUES	MULTI-THRESHOLD CMOS, SUPER-CUTOFF CMOS,ZIGZAQ,STACK EFFECT,LECTOR,SLEEPY STACK,SLEEPY KEEPER,DUAL SLEEP,SLEEPY-PASS GATE & TRANSISTOR GATING
13	JEFFERSON A HORA,NIEVAM MAPULA	For Ultra Low Power Application Design Of Rf To Dc Converter In 90nm Cmos Technology	Dec-2015	ULTRA LOW POWER	VOLTAGE RECTIFIER IS USED
14	MANAS SINGHAL,RAJESH MEHRA	Area Efficient Low Skewed Even Parity Generator Layout Development	Dec-2015	AREA EFFICIENCY	UNSKEWED & LOSKEWED TECHNIQUES
15	ANDRES GOMEZ,CHRISTIAN PINTO	Reducing Energy Consumption In Microcontroller-Based Platforms With Low Design Margin Co-Processors	Oct-2015	ENERGY MINIMIZATION TECHNIQUES	DVFS,THERMAL MANAGEMENT TECHNIQUES
16	SARANG KULKARNI,NEHA RAI	Minimizing Leakage Current Using Cmos Technology for a 0.25µm Scvl Based 4T Dram Design	Sep-2015	MINIMIZING LEAKAGE CURRENT	SELF CONTROLLABLE VOLTAGE LEVEL TECHNIQUE
17	XIAOZHE LIU, YONGAN ZHENG	For Chinese Uhf Rfid Transponder An Ultra Low Power Digital Processor	Oct-2015	LOW POWER BASE BAND PROCESSOR FOR UHF RFID TAG	HIGHLY REUSED REGISTER BANK , LOW FRQUENCY DECODING & SORT ALGORITHM

18	R VANITHA,S. THENMOZHI	Signal Processing Applications design using Low Power Cmos Comparator and Bipolar Cmos Technology	Aug-2015	ADC	SUPPLY BOOSTING,BODY-DRIVEN TRANSISTORS, CURRENT MODE DESIGN
19	JENIL,RAHUL	Design & Development Of Efficient Reversible Floating Point Arithmetic Unit	Nov-2015	REVERSIBLE FPAU	REVERSIBLE LOGIC,QUANTUM CIRCUIT
20	TOMOKI, SHINTARO	A Low Power 6t-4c Non Volatile Memory Using Charge Sharing & Non-Precharge Techniques	Mar-2015	FRAM	BITLINE NONPRECHARGE TECHNIQUE, PLATE LINE CHARGE SHARE TECHNIQUE
21	G KARTHIK REDDY	Low Power PTL based ALU design using LP- FA Design	Mar-2015	ALU DESIGN	PASS TRANSISTOR LOGIC
22	JAGADEEP KAUR, SHIWANI	Design Of Full Adder Circuit Using Double Gate Mosfet	Oct-2015	FULL ADDER	DOUBLE GATE PTL
23	BALAMURUGAN V	Performance Analysis of ADML using Leakage Power Reduction Techniques	Jun-2015	DYNAMIC POWER & LEAKAGE POWER	DUAL MODE LOGIC APPROACH
24	DANIEL,ALEXANDER	Intra-Operation Dynamic Voltage Scaling	Apr-2015	VOTAGE SCALING	INTRA OPERATION DYNAMIC VOLTAGE SCALING
25	HIPPOLYTE, BHEKISIPHO	Leakage Current Minimization & Power Reduction Techniques Using Sub-Threshold Design	Mar-2015	LEAKAGE POWER REDUCTION TECHNIQUES	SUBTHRESHOLD DESIGN

3. IMPLEMENTATION

The proposed work starts with single bit ALU and single bit power gated ALU, followed by the 4-bit ALU & 8-bit ALU implementations. Figure2 depicts the MOS model parameters used for the design.

Mos Model 3 parameters			
Parameter	Definition	Typical Value 0.12µm NMOS	pMOS
VTO	Theshold voltage of a long channel device, at zero Vbs.	0.4V	-0.4V
U0	Carrier mobility	0.06 m^2/V.s	0.025 m^2/V.s
TOX	Gate oxide thickness	3 nm	3 nm
PHI	Surface potential at strong inversion	0.3V	0.3V
LD	Lateral diffusion into channel	0.01µm	0.01µm
GAMMA	Bulk threshold parameter	0.4 $V^{0.5}$	0.4 $V^{0.5}$
KAPPA	Saturation field factor	0.01 V^{-1}	0.01 V^{-1}
VMAX	Maximum drift velocity	150Km/s	100Km/s
THETA	Mobility degradation factor	0.3 V^{-1}	0.3 V^{-1}
NSS	Substhreshold factor	0.07 V^{-1}	0.07 V^{-1}
W	MOS channel width	0.5-20µm	0.5-40µm
L	MOS channel length	0.12µm	0.12µm

Figure 2. MOS model3 parameters for 120nm.

Power gating is effective in reducing power consumption. Power gating is a technique that temporarily shuts down unused circuit blocks to reduce overall chip leakage. This temporary shutdown time is also called "sleep mode" or "inactivity mode". When circuit blocks are needed again for operation, they are activated into "active mode". These two modes are switched at the right time and in the right manner to maximize power performance with minimal performance impact. Therefore, the purpose of power gating is to minimize power leakage by temporarily removing power to selected blocks that are not needed in this mode. Power gating has a greater impact on design architecture than clock gating. The time delay is increased due to the need to safely enter and exit power gated mode. The amount of leakage power savings possible in such low-power modes and the energy dissipation to enter and exit such modes leads to several architectural tradeoffs. Block shutdown can be done in software or hardware. Driver software can schedule shutdown events. You can use a hardware timer. A dedicated power management controller is another option. Power gating uses low-leakage PMOS transistors as header switches to turn off parts of the design in standby or sleep mode. An NMOS footswitch can also be used as a sleep transistor. The insertion of sleep transistors divides the chip's power grid into a permanent power grid connected to the power supply and a virtual power grid that drives the cells and can be switched off. The quality of this complex power grid is critical to a successful power gating design. Two of the most important parameters are IR drop and the cost of silicon area and routing resources. Power gating can be implemented using a cell or cluster-based (or fine-grained) approach, or a distributed coarse-grained approach. Successful implementation of this methodology requires consideration of the following parameters and careful selection of their values. Power Gate Size, Gate Controlled Slew Rate, Simultaneous Switching Capacitance, Power Gate Leakage, Fine Grain Power Gating, Coarse Grain Power Gating.
The ALU performs the basic operations of Add, Sub, Or, And & NOP with the combinations od selection lines S0,S1 respectively. Power gating technique with fine grain methodology is employed as shown in figure 2a.

ISSN NO: 2230-5807

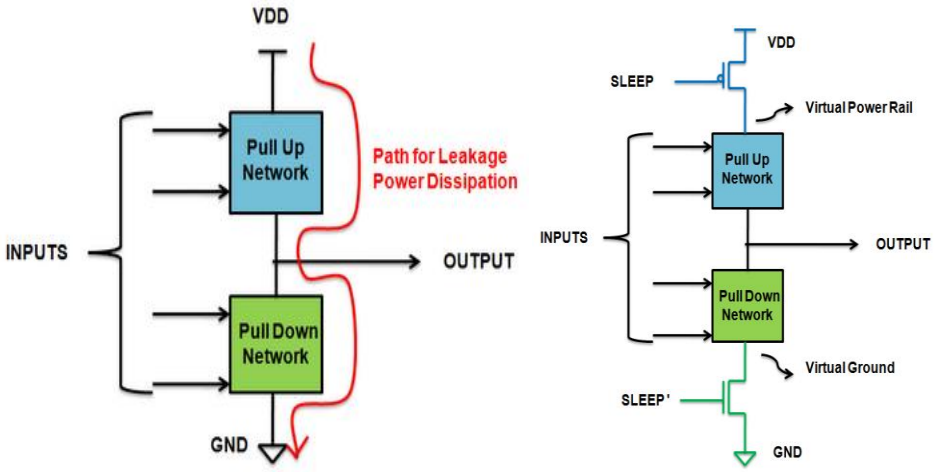

Figure 2a. Sleep transistors operation.

The proposed design of single bit ALU is shown in fig3 and power gated single bit ALU is shown in fig 6.

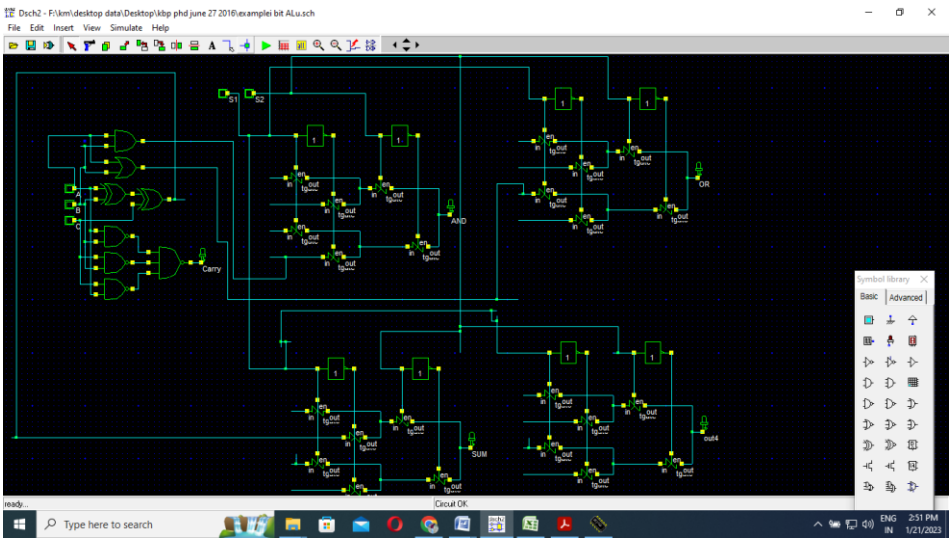

Figure 3. Schematic of Single bit ALU

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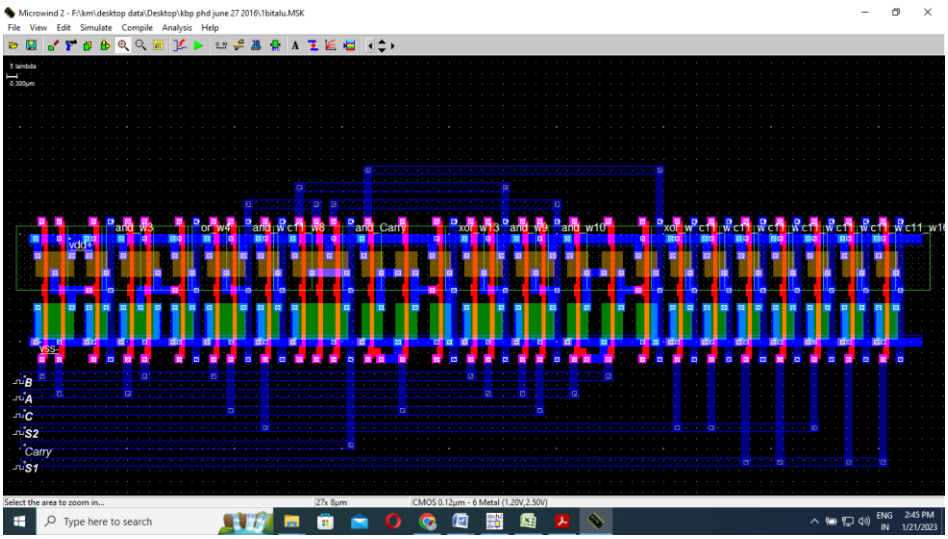

Figure 4. Layout of Single bit ALU

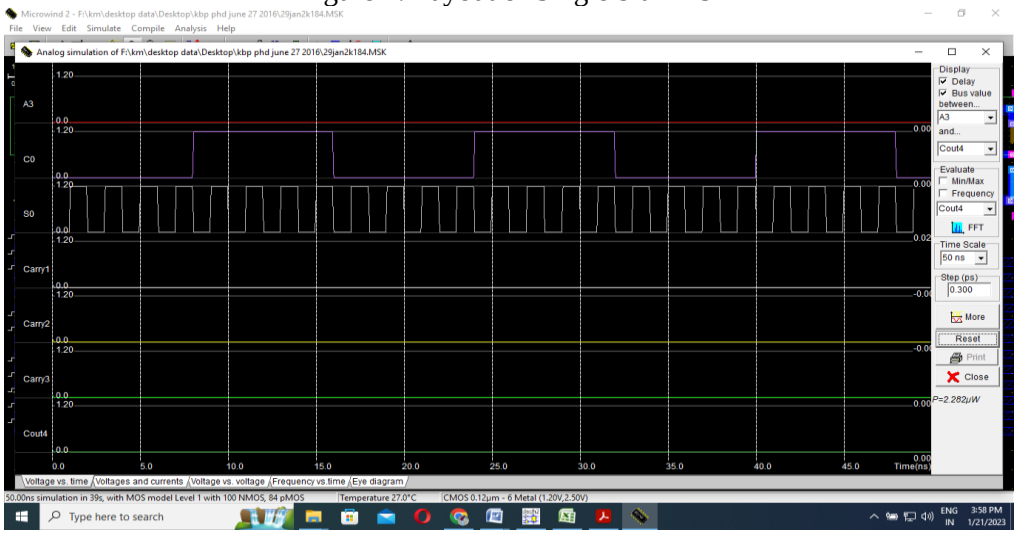

Figure 5. Timing diagram of Single bit ALU

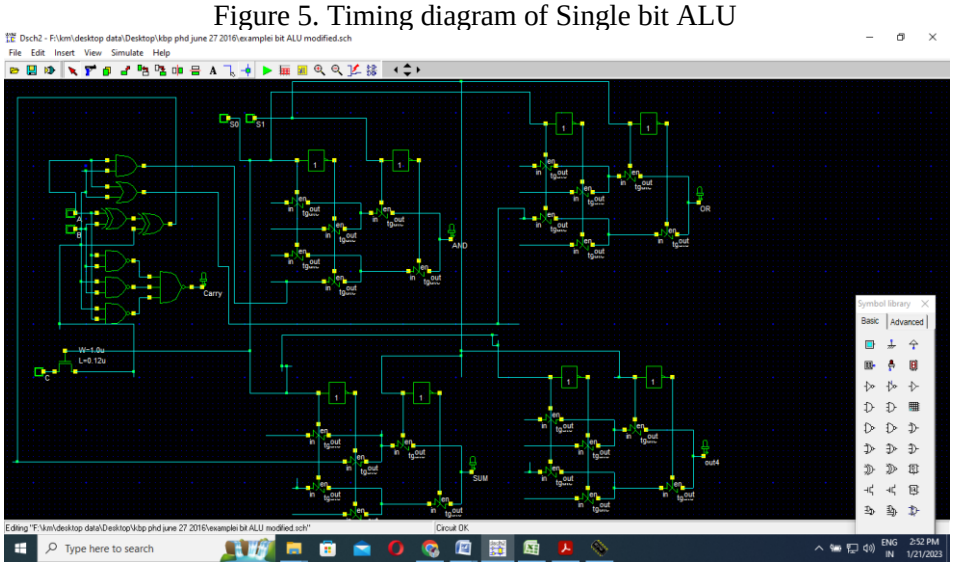

Figure 6. Schematic of Power-gated Single bit ALU

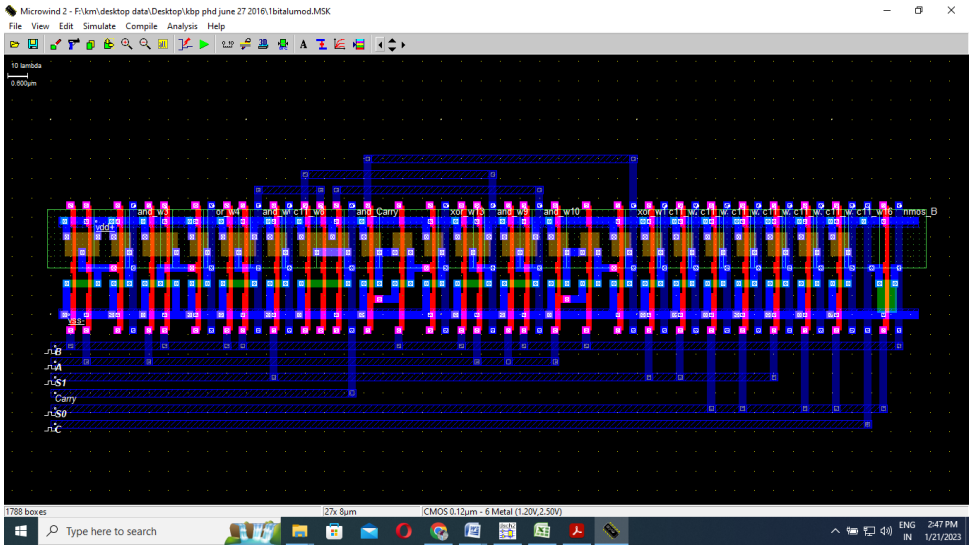

Figure 7. Layout of Power gating Single bit ALU

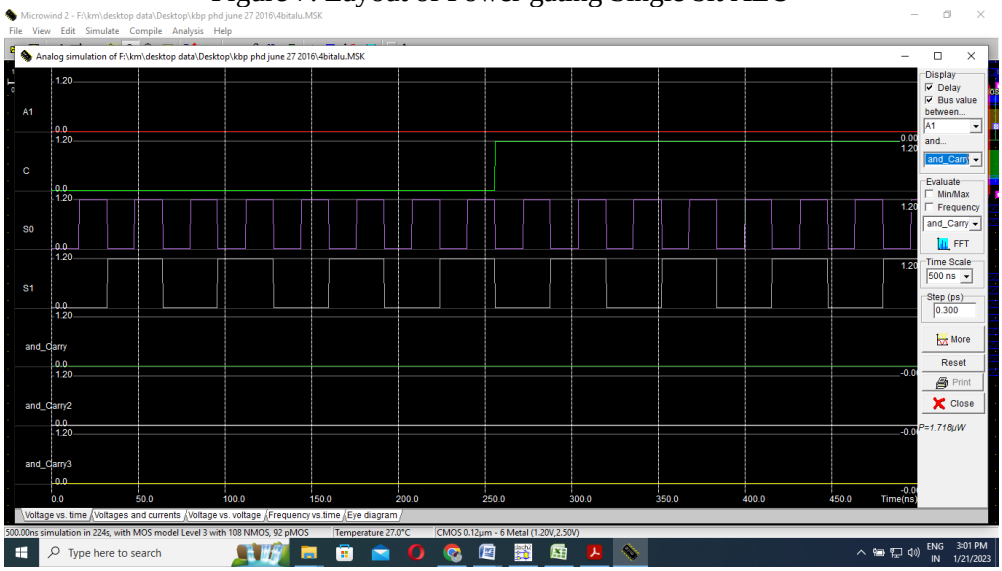

Figure 8. Timing diagram of Power gating Single bit ALU

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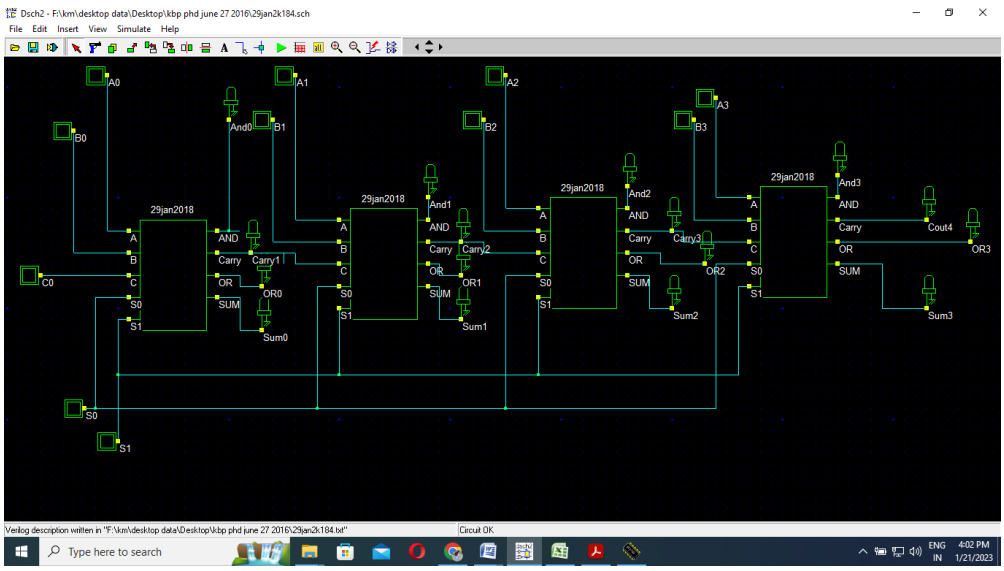

Figure 9. Schematic of Four bit Normal ALU

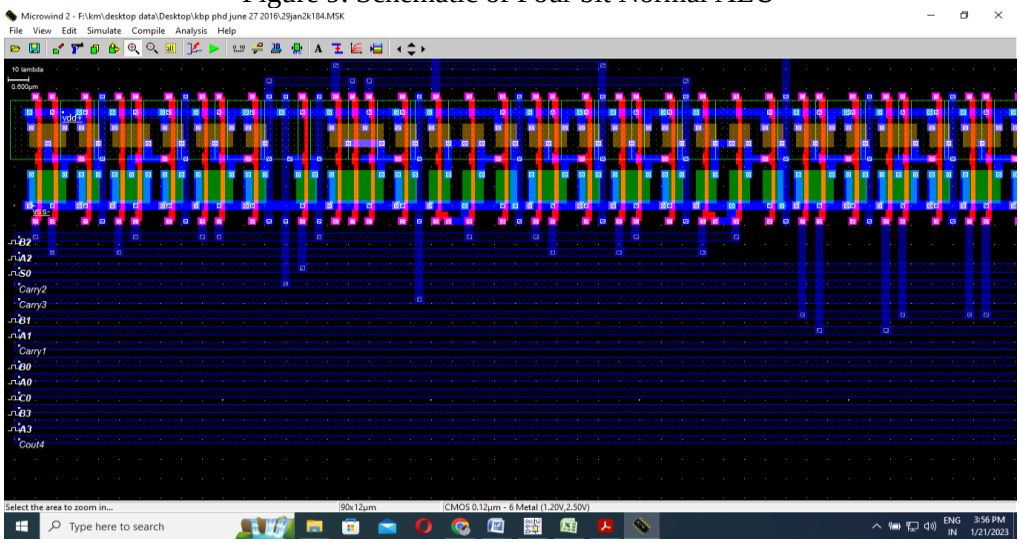

Figure 10. Layout of Normal Four bit ALU

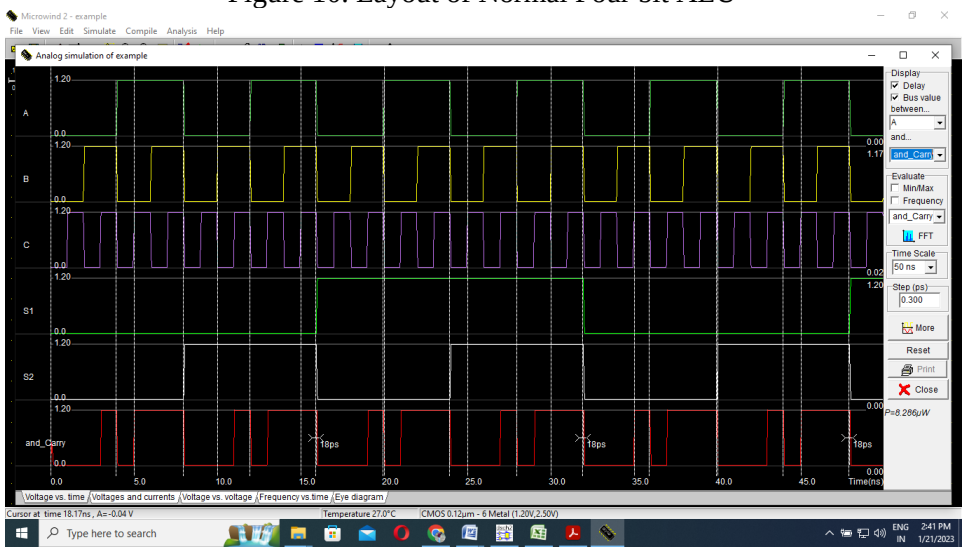

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Figure 11. Timing diagram of Normal Four bit ALU

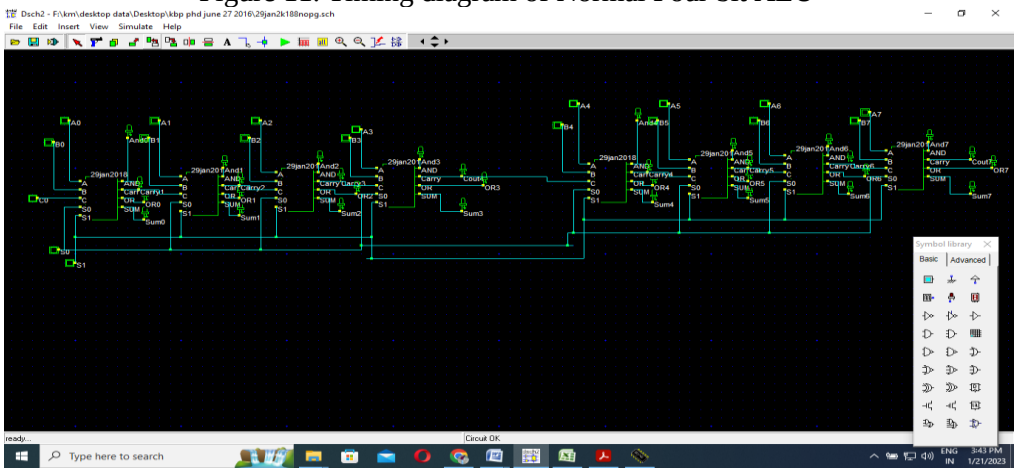

Figure 12. Schematic diagram of Normal Eight bit ALU

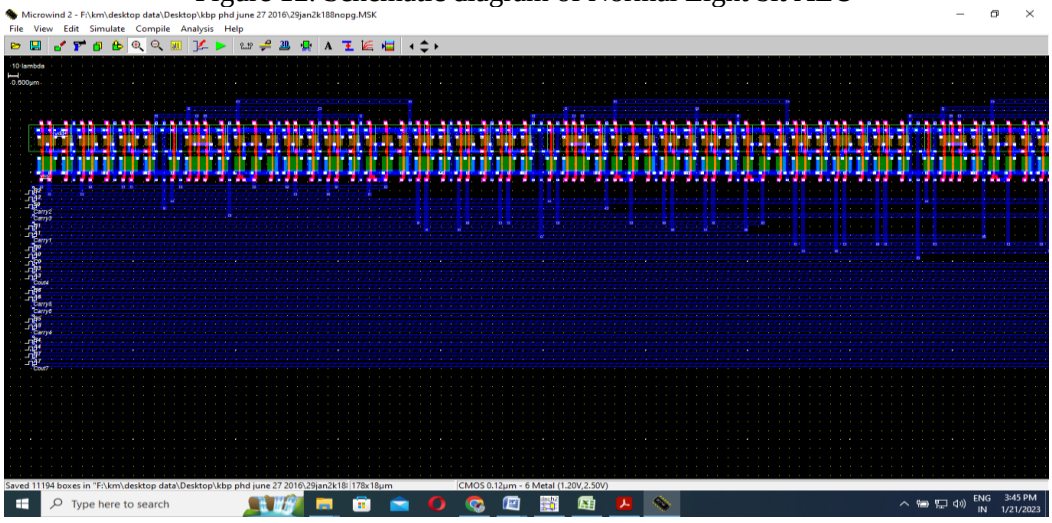

Figure 13. Layout of Normal Eight bit ALU

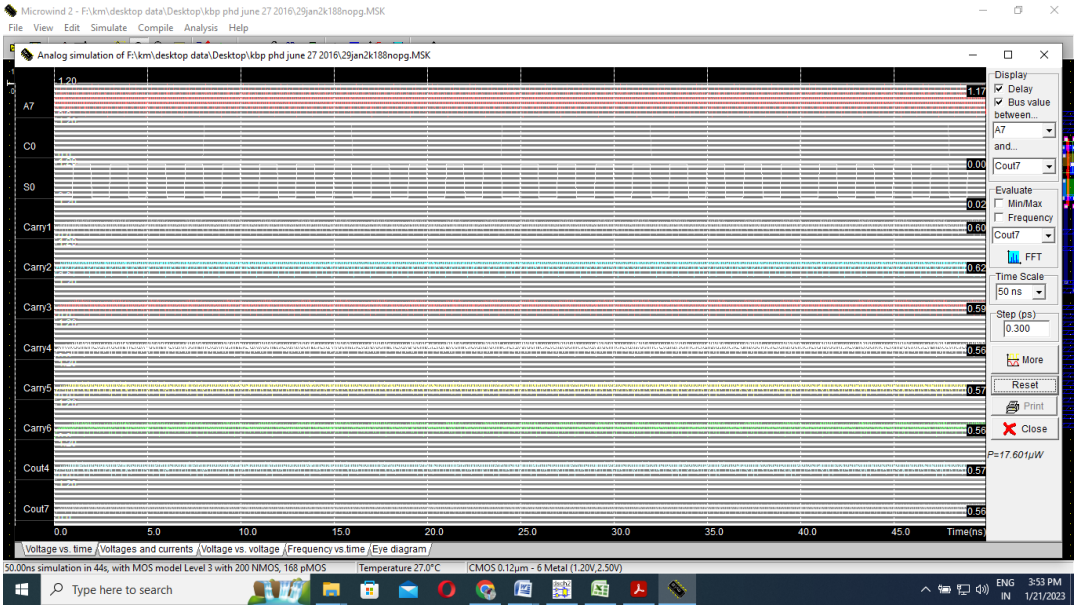

Figure 14. Timing diagram of Normal Eight bit ALU

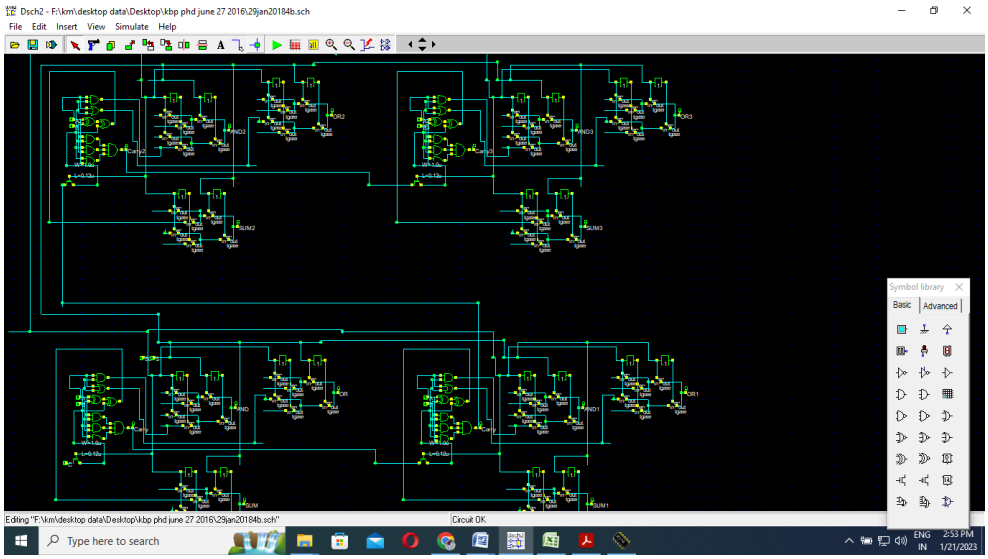

Figure 15. Schematic of Four bit Power gating ALU

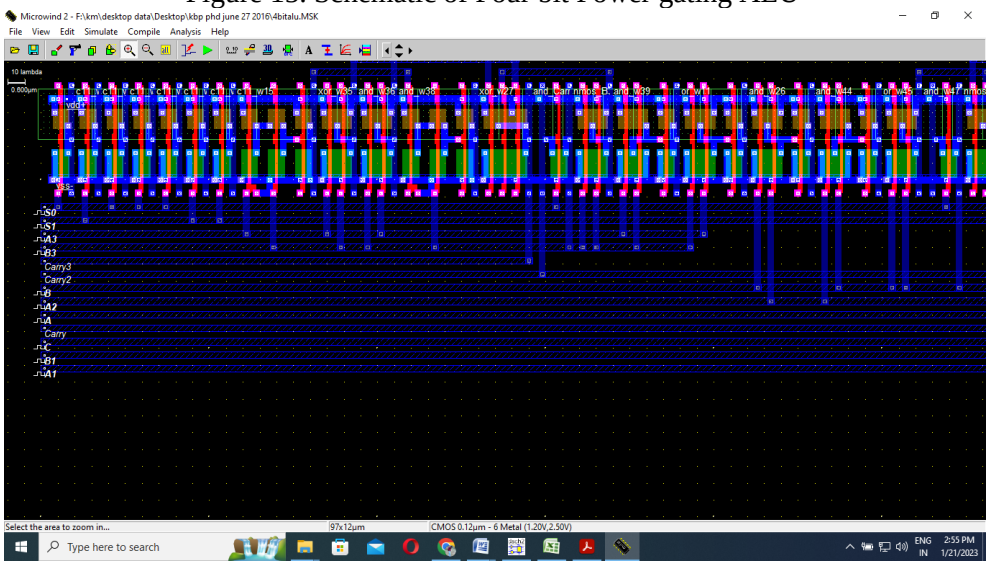

Figure 16. Layout of Power gating four bit ALU

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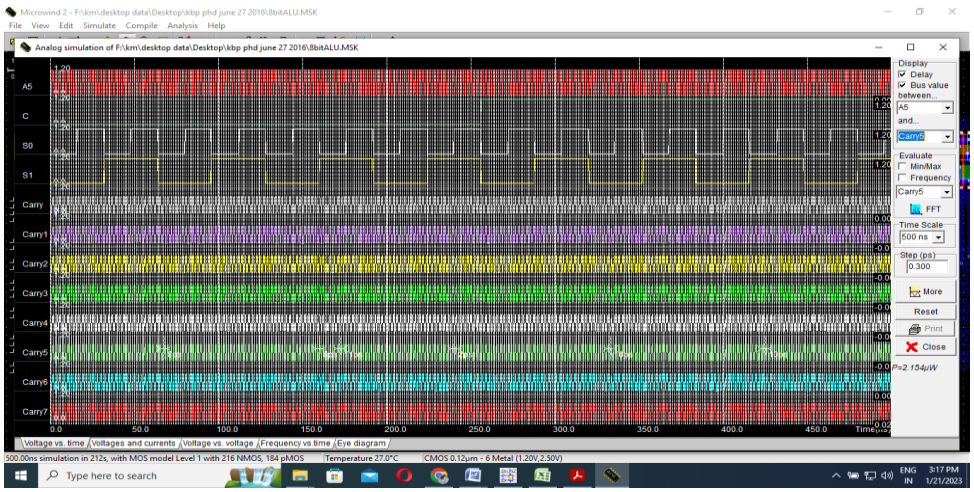

Figure 17. Timing diagram of Power gating Four bit ALU

Figure 18. Schematic of Eight bit Power gating ALU

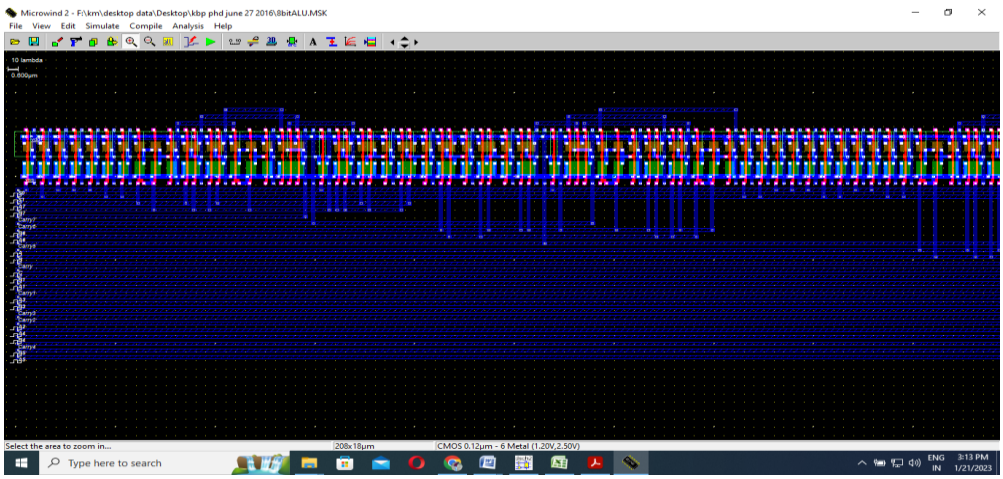

Figure 19. Layout of Power gating Eight bit ALU

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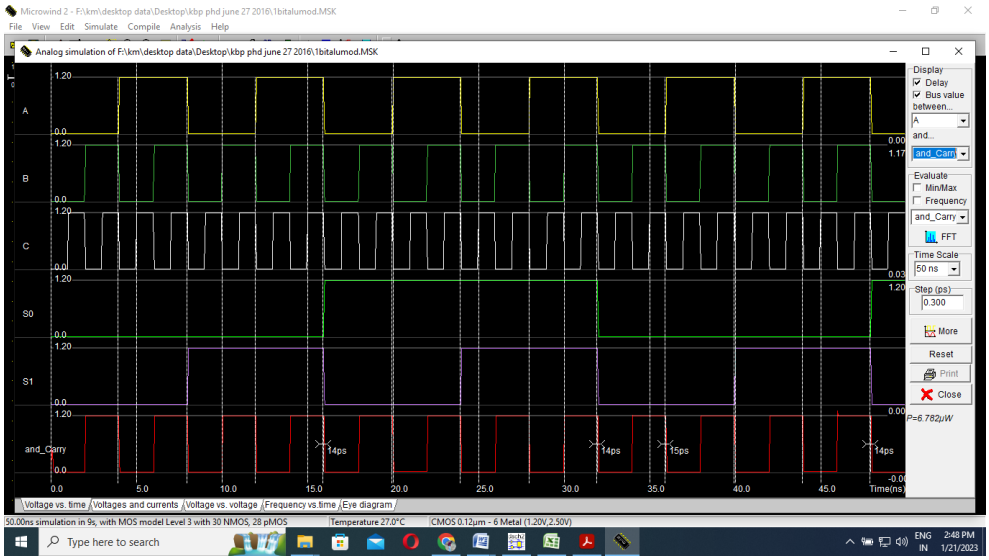

Figure 20. Timing diagram of Power gating Eight bit ALU

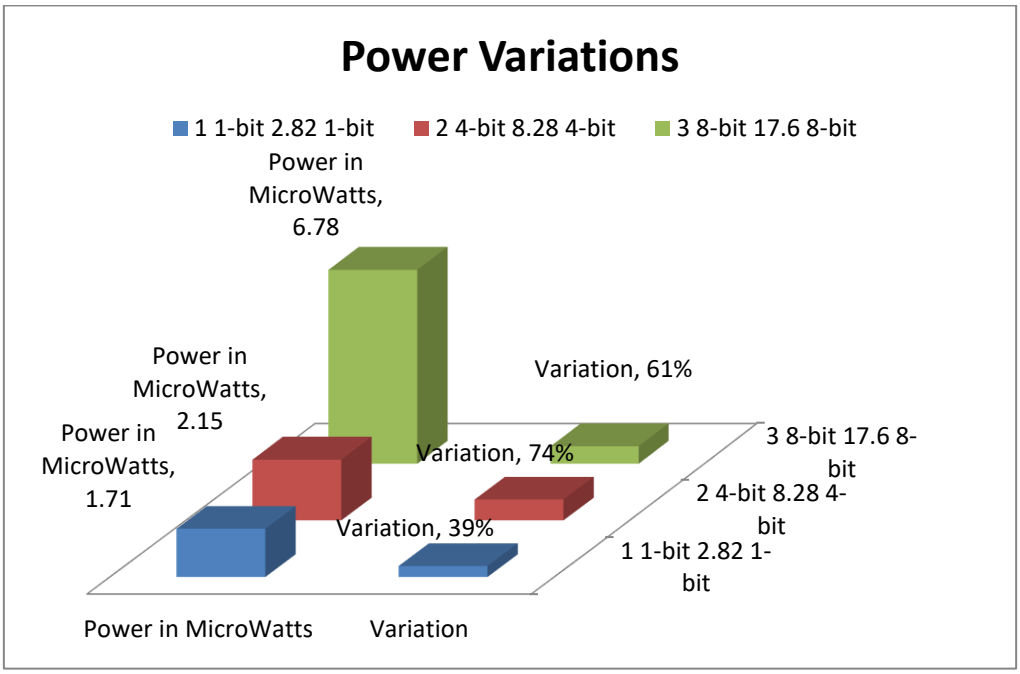

Figure 21. Power dissipation comparisons in µW of Power Gated & Normal ALU

CONCLUSIONS

In the proposed design the power dissipations are obtained with 120nm mos3 model files and the tabular form is shown below table3.

Sl.No	NORMAL-ALU	Power in MicroWatts	POWERGATED-ALU	Power in MicroWatts	Variation
1	1-bit	2.82	1-bit	1.71	39%

2	4-bit	8.28	4-bit	2.15	74%
3	8-bit	17.6	8-bit	6.78	61%

We can conclude that for power-gated ALU design there is around 39-77% variations in power dissipation. In future we can use more number of add-on functions to the ALU and can be effectively replaced with Reversible logic gates, Finfet gates.

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[25] HIPPOLYTE,BHEKISIPHO LEAKAGE CURRENT MINIMISATION & POWER REDUCTION TECHNIQUES USING SUB-THRESHOLD DESIGN 3/1/15 IEEE XPLORE 146-150

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